UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,854	09/05/2003	Rafael Reif	MIT-136AUS	7254

22494 7590 05/28/2009

DALY, CROWLEY, MOFFORD & DURKEE, LLP
SUITE 301A
354A TURNPIKE STREET
CANTON, MA 02021-2714

EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
05/28/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@dc-m.com
amk@dc-m.com

Office Action Summary	Application No.	Applicant(s)	
	10/655,854	REIF ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/11/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8, 10-40, 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-40 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/1409&1/15/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The request for reconsideration filed on 02/12/2007 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, 4-8, 10-13 and 17-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyanagi et al. (US 6,525,415; US2001/0005059(prior publication)) in view of Hubner (US 5,706,578).

6. Regarding claims 1 and 17, Koyagani (e.g. figs. 1 & 5) shows a multi layer integrated semiconductor structure, comprising:

a) at least a first device layer 40 having first and second opposing surface, the firs device layer includes:

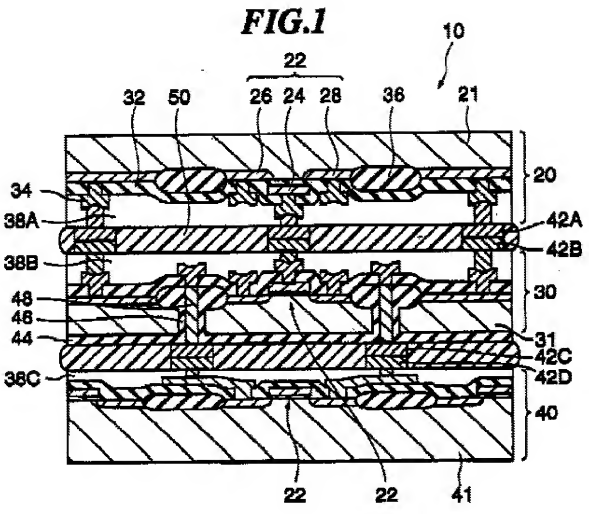
- A first substrate 40 having a first surface corresponding to the first surface of the first device layer and having a second opposite surface, the first substrate having provided therein at lest a first doped region 26/28 which forms at least part of one or more semiconductor elements 22 (e.g. source/drain);
- A first dielectric layer 32/38 having first and second opposing surfaces with the first dielectric material surface disposed about the first doped semiconductor region and wherein the second surface of the first dielectric material correspond to the second surface of the first device layer, the dielectric material having at least a first via hole with a first conductive material 34a disposed therein to provide a first conductive via having first and second opposing ends with a first one of the first and second ends of the first conductive via electrically coupled to at least a portion of the at least one of the one or more semiconductor elements and a second one of the first

and second ends of the first conductive via exposed through the second surface of the first dielectric material;

b) at least a second device layer 30 having first and second opposing surfaces, with the first surface of the device layer including.

- a second substrate 31 having first and second opposing surface and having provided therein at least a second doped semiconductor region (source/drain) which forms at least part of one or more semiconductor elements 22;
- and a second dielectric material 32/38 having firs and second opposing surfaces with the first dielectric material surface is disposed about the second doped semiconductor region and the second surface of the second dielectric material corresponding to the second surface of the second device layer and wherein the second substrate includes a second via hole having a second conductive material 48 disposed therein to provide a second conductive via having first and second ends with a first one of the first and second ends of the second conductive via electrically coupled to at least a portion of at least one of the one or more semiconductor element of the second substrate and a second one of the first and second ends of the second conductive via is exposed though the second surface of the second dielectric layer; and

c) a first conductive interface 42 having a first surface and a second opposing surface with the first surface of the conductive interface disposed between at least a portion of a first one of the first and second opposing surfaces of the first device layer and at least a portion of a first one of the first and second opposing surfaces of the second device layers such that it electrically couples the first device layer to the second device layer wherein the conductive interface and the first and second conductive vias form at least a portion of an electrical communication path between the first device layer and the second device layer (see also fig. 5).



Although it is implicit in the disclosure that at least a portion of the first conductive interface secures together the first and second device layers, this limitation is not explicitly taught. However, Hubner (e.g. fig. 1) teaches an analogous structure of that disclosed by Koyanagi including a conductive interface having a solder 25 securing a first and a second device. It would have been obvious to one of ordinary skills in the art to make the first conductive interface disclosed by Koyanagi including a solder as

disclosed by Hubner to provide a firm joint between the first and the second device layer (col. 1/ll. 58-60)

7. Regarding claim 2, Koyanagi shows a first conductive interconnect element 34b disposed in the dielectric material of the first device layer with a first end of the conductive interconnect element coupled to the first conductive via and a second end of the first conductive interconnect element coupled to at least one of the first plurality of doped semiconductor elements.

8. Regarding claim 4, Koyanagi shows a second conductive interconnect 34c having a first portion disposed over at least a portion of one of the second plurality of doped regions and having a second portion electrically coupled to the second end of the second conductive via.

9. Regarding claim 5, Koyanagi shows a second conductive interconnect 34c disposed in the second device layer and coupled to the second conductive via provided in the second device layer.

10. Regarding claim 6, Koyanagi shows that the second conductive interconnect is coupled to at least one of the semiconductor element of the second device layer.

11. Regarding claim 7, Koyanagi shows that the second conductive via includes a first end electrically coupled to the at least one of the one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface.

12. Regarding claim 8, Koyanagi shows that the second device layer comprises a second conductive interconnect 34c having a first portion electrically coupled to the

second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive vias to the at least one element of the second plurality of semiconductor elements.

13. Regarding claim 10, Koyanagi shows a third conductive via 34b provided in the first device layer, wherein the third conductive via is coupled between a portion of the first conductive interconnect and the at least one of the first plurality of doped regions.

14. Regarding claim 11, Koyanagi shows a second conductive interface 42 disposed over a first surface of the second device layer and, wherein the second conductive via forms at least a part of the electrical communication path between the second conductive interconnect and the second interface.

15. Regarding claim 12, Koyanagi shows that the first conductive via forms at least a signal path between the conductive interface and at least one of the first and second plurality of semiconductor elements.

16. Regarding claim 13, Koyanagi shows that the second end of the first conductive via is coupled to the at least one element of the first plurality of semiconductor elements.

17. Regarding claim 18, Koyanagi shows a first conductive interconnect element 34b disposed in the first layer with a first portion of the first conductive via electrically coupled to at least a portion of the first conductive interconnect element and a second portion of the first conductive interconnect element coupled to the first doped semiconductor region.

18. Regarding claims 19, Koyanagi shows that the first conductive via couples the first conductive interconnect element to the first conductive interface.

19. Regarding claim 20, Koyanagi shows that the second conductive via is formed on the first one of the first and second opposing surfaces of the second device layer and is electrically coupled to the second doped semiconductor region (abstract).

20. Regarding claim 21, Koyanagi shows a third conductive via coupled to the second doped semiconductor region (e.g. see connection plug 34c)

21. Regarding claim 22, Koyanagi shows a second conductive interface 42 disposed on the second one of the first and second opposing surfaces of the second device layer and wherein a third conductive via 34a is provided having a first end coupled to the second doped semiconductor region and a second end coupled to the second conductive interface.

22. Regarding claim 23, Koyanagi shows that the second conductive via is formed on the first one of the first and second opposing surface of the second device layer and wherein the second device layer comprises a first conductive interconnect.

23. Regarding claim 24, Koyanagi shows that the second conductive via is provided having a first end coupled to the conductive interconnect and a second end coupled to the fist conductive interface.

24. Regarding claim 25, Koyanagi shows that the first conductive via is coupled to at least the first doped semiconductor region.

25. Regarding claim 26, Koyanagi shows that the first conductive via is provided having a first end coupled to at least the first doped semiconductor region and a second end coupled to the first conductive interface.

26. Regarding claim 27, Koyanagi shows that the first interface corresponds to a first conductor interface region. Also, a second interface region 50 is disposed between the first one of the first and second device layers with the second interface region provided from a non-conductive material.

27. Regarding claim 28, Koyanagi shows that the first conductive interface region is provided from a conductive bonding material (col. 7/lls. 1-5).

28. Regarding claim 29, Koyanagi shows a second conductive interconnect element (source/drain contact plug) disposed in the second device layer with a portion of the second conductive interconnect element coupled to the second conductive via and wherein the first conductive via, the first conductive interface and the second conductive via provide a direct vertical electrical connection between the first conductive interconnect element and the second conductive interconnect element.

29. Regarding claim 30, Koyanagi shows that the first device layer is constructed and arranged to operate using at least one of electronic components (abstract).

30. Regarding claim 31, Koyanagi shows that the second device layer is constructed and arranged to operate using at least one of electronic components (abstract).

31. Regarding claim 32, Koyanagi shows that the first device layer includes a transistor.

32. Regarding claim 33, Koyanagi shows that the second device layer includes a transistor.

33. Regarding claims 34 and 35, Koyanagi shows that the first and second device layers includes a die element (transistor) located on a wafer (col. 11/lls. 29-30).

34. Regarding claim 36, Koyanagi shows that the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area differs from the second predetermined surface area.

35. Regarding claim 37, Koyanagi shows that the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area is substantially equivalent to the first predetermined surface area.

36. Regarding claim 38, Koyanagi shows a first conductive interconnect element (e.g. wiring) having a first portion coupled to the first doped semiconductor region, and a second portion coupled to a first end of the first conductive via.

37. Regarding claim 39, Koyanagi shows a second conductive interconnect element (e.g. plug) having a first portion coupled to the second doped semiconductor region and a second portion coupled to a first end of the second conductive via with the second end of the first conductive via and the second end of the second conductive via each coupled to the first interface.

38. Regarding claims 40 and 42, Koyanagi (e.g. figs. 1 & 5) shows a multi-layer semiconductor structure, comprising: a first semiconductor wafer 40 having first and

second opposing surfaces, the first semiconductor wafer including a first plurality of semiconductor structures each of which includes a first plurality of semiconductor elements 22, the first semiconductor wafer also comprising a first plurality of conductive vias 34b, at least some of the first plurality of conductive vias disposed such that a first end of thereof is electrically coupled to at least one of the first plurality of semiconductor elements and a second is exposed through one of the first and second surfaces of the first semiconductor wafer; a second semiconductor wafer 30 having first and second opposing surfaces, the second semiconductor wafer including a second plurality of semiconductor structures each of which includes a second plurality of semiconductor elements 22, the second semiconductor wafer also comprising a second plurality of conducive vias 48 disposed such that a first end of thereof is electrically coupled to at least some of the second plurality of second elements and a second end is exposed though one of the first and second surfaces of the semiconductor wafer; and at least a first conductive interface segment 42 disposed between a first one of the first and second opposing surfaces of the first semiconductor wafer and a first one of the first and second opposing surfaces of the second semiconductor wafer, the first conductive interface segment disposed over at least a first one of the plurality of semiconductor structures of the first semiconductor wafer and being in an electrical communication relationship though the first plurality of conductive vias electrically coupled to the first plurality of semiconductor elements with at least a first one of the first plurality of the semiconductor elements of the first semiconductor structure and at least a first one of the plurality of semiconductor elements of the second semiconductor structure of the

second semiconductor wafer where the first conductive interface segment and at least some of the first and second plurality of conductive vias form electrical signal paths between at least some of the first semiconductor elements of the first semiconductor structure and at least some of the second semiconductor elements of the second semiconductor structure. Although it is implicit in the disclosure that at least a portion of the first conductive interface secures/bonds together the first and second device layers, this limitation is not explicitly taught. However, Hubner (e.g. fig. 1) teaches an analogous structure of that disclosed by Koyanagi including a conductive bonding interface having a solder/bonding material 25 securing a first and a second device. It would have been obvious to one of ordinary skills in the art to make the first conductive interface disclosed by Koyanagi as the first conducting bonding interface disclosed by Hubner to provide a firm joint between the first and the second device layer (col. 1/ll. 58-60)

39. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Koyanagi et al. (US 6,525,415; US2001/0005059) in view of in view of Hubner (US 5,706,578) further in view of Nulman (US 5,904,562).

40. Regarding claim 14, Koyanagi in view of Hubner shows most aspects of the instant invention except for the use of copper to make the first conductive interface. Nevertheless, Nulman teaches that copper is a suitable material to make metallization films (col. 1/lls. 28-38). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the first conductive interface (film metallization) disclosed by Koyanagi in view of Hubner of copper as taught by Nulman,

since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

41. Regarding claim 15, Koyanagi shows that the conductive interface is provided as a first conductive interface region and the multi layer integrated semiconductor structure further comprises a second conductive interface region 42 disposed between the first and second device layers with the second conductive interface region being physically separated from the first conductive interface region.

42. Regarding claim 16, Koyanagi teaches that the second interface region includes an adhesive material such that the second interface region secures the first device layer to the second device layer (col. 7/lls. 1-5).

Response to Arguments

43. Applicant's arguments with respect to have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andújar
Primary Examiner
Art Unit 2826

/Leonardo Andújar/
Primary Examiner, Art Unit 2826